Abstracts

A 2.7 V mixed signal processor for CDMA/AMPS cellular phones

Z.M. Shi, O. Salminen, K. Hsu, M. Wang, S. Maire, J. Vahe, E. Malo, E. Erkkila, J.M. Heikkila and K. Kaltiokallio. "A 2.7 V mixed signal processor for CDMA/AMPS cellular phones." 1999 Radio Frequency Integrated Circuits (RFIC) Symposium 99. (1999 [RFIC]): 29-32.

This paper describes the design approach and test results of a monolithic mixed signal processor for use in dual-mode CDMA/AMPS (IS-95A) cellular phones. The processor interfaces between RF and digital baseband blocks. It comprises of a low jitter 9.8 MHz PLL, a high speed 4/8-bit CDMA/AMPS codec, channel filters, a 12-bit FM demodulator, a low power 13-bit voice codec and speech filters. The processor design is targeted for low power applications and fabricated in a low power 0.5 /spl mu/m CMOS technology. The statistical test results measured from -30/spl deg/C to +85/spl deg/C with a standard process variation demonstrate that the system completely fulfils IS-98A CDMA handset performance specification.

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